IN THE CLAIMS

No claims are amended, added or canceled herein. The presently-pending claims, along with their status identifiers, are provided below.

1. (Original) A gate stack, comprising:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

2. (Original) The gate stack of claim 1, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

3. (Withdrawn) The gate stack of claim 1, wherein the tunnel medium is disposed on the injector medium.

4. (Original) The gate stack of claim 1, wherein the tunnel medium includes tunnel Al_2O_3.

5. (Withdrawn) The gate stack of claim 1, wherein the tunnel medium includes tunnel SiO_2.

6. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

7. (Canceled)

8. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes tantalum.

9. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes titanium.

10. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes zirconium.

11. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes hafnium.

12. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes praseodymium.

13. (Withdrawn) The gate stack of claim 1, wherein the high K charge blocking and charge storing medium includes BST.

14. (Original) The gate stack of claim 1, wherein the injector medium includes injector SRN.

15. (Withdrawn) The gate stack of claim 1, wherein the injector medium includes injector SRO.

16. (Withdrawn) The gate stack of claim 1, wherein the injector medium includes silicon rich aluminum nitride.

17. (Withdrawn) The gate stack of claim 1, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

18. (Original) A gate stack, comprising:
a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes nano crystals for providing charge trapping charge centers; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

19. (Original) The gate stack of claim 18, wherein the nano crystals include silicon nano crystals.

20. (Withdrawn) The gate stack of claim 18, wherein the nano crystals include gold nano crystals.

21. (Withdrawn) The gate stack of claim 18, wherein the nano crystals include tungsten nano crystals.

22. (Withdrawn) The gate stack of claim 18, wherein the nano crystals include silicided nano crystals.

23. (Withdrawn) A gate stack, comprising:

a first injector medium;

a tunnel medium disposed on the first injector medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

a second injector medium disposed on the high K charge blocking and charge storing medium.

24. (Withdrawn) The gate stack of claim 23, wherein the first injector medium is disposed on a NO surface treated substrate.

25. (Withdrawn) The gate stack of claim 23, wherein the first injector medium is disposed on a NH_3 surface treated substrate.

26. (Withdrawn) The gate stack of claim 23, wherein the tunnel medium is selected from the group consisting of tunnel Al_2O_3 and tunnel SiO_2.

27. (Withdrawn) The gate stack of claim 23, wherein the injector medium is selected from the group consisting of injector SRN, injector SRO, and silicon rich aluminum nitride.

28. (Withdrawn) The gate stack of claim 23, wherein the high K charge blocking and charge storing medium includes Al_2O_3.

29. (Withdrawn) A gate stack, comprising:

a first injector medium;

a tunnel medium disposed on the first injector medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes nano crystals for providing charge trapping charge centers; and

a second injector medium disposed on the high K charge blocking and charge storing medium.

30. (Withdrawn) The gate stack of claim 29, wherein the nano crystals include silicon nano crystals.

31. (Withdrawn) The gate stack of claim 29, wherein the nano crystals include gold nano crystals.

32. (Withdrawn) The gate stack of claim 29, wherein the nano crystals include tungsten nano crystals.

33. (Withdrawn) The gate stack of claim 29, wherein the nano crystals include silicided nano crystals.

34. (Withdrawn) A gate stack, comprising:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

35. (Withdrawn) The gate stack of claim 34, wherein the injector medium is disposed on the high K charge blocking medium.

36. (Withdrawn) The gate stack of claim 34, wherein the tunnel medium is disposed on the injector medium.

37. (Withdrawn) The gate stack of claim 34, wherein the tunnel medium is selected from the group consisting of tunnel Al_2O_3 and tunnel SiO_2.

38. (Withdrawn) The gate stack of claim 34, wherein at least one of the high K charge blocking and the high K charge storing medium is selected from the group consisting of Al_2O_3, tantalum, titanium, zirconium, hafnium, praseodymium and BST.

39. (Withdrawn) The gate stack of claim 34, wherein the injector medium is selected from the group consisting of injector SRN, injector SRO, and silicon rich aluminum nitride.

40. (Withdrawn) The gate stack of claim 34, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

41. (Withdrawn) A gate stack, comprising:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes nano crystals for providing charge trapping charge centers;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

42. (Withdrawn) The gate stack of claim 41, wherein the nano crystals include silicon nano crystals.

43. (Withdrawn) The gate stack of claim 41, wherein the nano crystals include gold nano crystals.

44. (Withdrawn) The gate stack of claim 41, wherein the nano crystals include tungsten nano crystals.

45. (Withdrawn) The gate stack of claim 41, wherein the nano crystals include silicided nano crystals.

46. (Withdrawn) A gate stack, comprising:

a first injector medium disposed on a substrate;

a tunnel medium disposed on the first injector medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium stored on the high K charge storing medium; and

a second injector medium disposed on the high K charge blocking medium.

47. (Withdrawn) The gate stack of claim 46, wherein the gate stack is disposed on a NO surface treated substrate.

48. (Withdrawn) The gate stack of claim 46, wherein the gate stack is disposed on a NH_3 surface treated substrate.

49. (Withdrawn) The gate stack of claim 46, wherein the first and second injector media include injector SRN.

50. (Withdrawn) The gate stack of claim 46, wherein the first and second injector media include injector SRO.

51. (Withdrawn) The gate stack of claim 46, wherein the first and second injector media include silicon-rich aluminum nitride.

52. (Withdrawn) The gate stack of claim 46, wherein the high K charge storing medium includes silicon nano crystals.

53. (Withdrawn) The gate stack of claim 46, wherein the high K charge storing medium includes gold nano crystals.

54. (Withdrawn) The gate stack of claim 46, wherein the high K charge storing medium includes tungsten nano crystals.

55. (Withdrawn) The gate stack of claim 46, wherein the high K charge storing medium includes silicided tungsten nano crystals.

56. (Original) A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

57. (Original) The memory cell of claim 56, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

58. (Withdrawn) The memory cell of claim 56, wherein the tunnel medium is disposed on the injector medium.

59. (Original) The memory cell of claim 56, wherein the tunnel medium includes tunnel Al_2O_3.

60. (Withdrawn) The memory cell of claim 56, wherein the tunnel medium includes tunnel SiO_2.

61. (Withdrawn) The memory cell of claim 56, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

62. (Canceled)

63. (Original) The memory cell of claim 56, wherein the injector medium includes injector SRN.

64. (Withdrawn) The memory cell of claim 56, wherein the injector medium includes injector SRO.

65. (Withdrawn) The memory cell of claim 56, wherein the injector medium includes silicon rich aluminum nitride.

66. (Withdrawn) The memory cell of claim 56, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

67. (Withdrawn) A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

68. (Withdrawn) The memory cell of claim 67, wherein the injector medium is disposed on the high K charge blocking medium.

69. (Withdrawn) The memory cell of claim 67, wherein the tunnel medium is disposed on the injector medium.

70. (Withdrawn) The memory cell of claim 67, wherein the tunnel medium includes tunnel Al_2O_3.

71. (Withdrawn) The memory cell of claim 67, wherein the tunnel medium includes tunnel SiO_2.

72. (Withdrawn) The memory cell of claim 67, wherein at least one of the high K charge blocking and the high K charge storing medium includes Al_2O_3.

73. (Original) A nonvolatile memory device, comprising:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

74. (Original) The nonvolatile memory device of claim 73, wherein the injector medium is disposed on the high K charge blocking and charge storing medium.

75. (Withdrawn) The nonvolatile memory device of claim 73, wherein the tunnel medium is disposed on the injector medium.

76. (Original) The nonvolatile memory device of claim 73, wherein the tunnel medium includes tunnel Al_2O_3.

77. (Withdrawn) The nonvolatile memory device of claim 73, wherein the tunnel medium includes tunnel SiO_2.

78. (Withdrawn) The nonvolatile memory device of claim 73, wherein the high K charge blocking and charge storing medium includes a high K charge blocking medium disposed on a high K charge storing medium with nano crystals.

79. (Canceled)

80. (Original) The nonvolatile memory device of claim 73, wherein the injector medium includes injector SRN.

81. (Withdrawn) The nonvolatile memory device of claim 73, wherein the injector medium includes injector SRO.

82. (Withdrawn) The nonvolatile memory device of claim 73, wherein the injector medium includes silicon rich aluminum nitride.

83. (Withdrawn) The nonvolatile memory device of claim 73, wherein the tunnel medium, the high K charge blocking and charge storing medium, and the injector medium are scalable with power supply and lithography scaling.

84. (Original) An electronic system, comprising:

a processor; and

a nonvolatile memory device coupled to the processor, the nonvolatile memory device including:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

85-116. (Canceled)

117. (Withdrawn) An electronic system, comprising:

a plurality of fixed threshold devices for performing random logic functions; and

a plurality of nonvolatile devices operably coupled to the plurality of fixed threshold devices to provide desired logic functions, wherein each of the plurality of nonvolatile devices includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

118. (Withdrawn) The electronic system of claim 117, wherein the plurality of fixed threshold devices include an input node, and the plurality of nonvolatile devices are operably coupled to the input node to provide the desired logic functions.

119. (Withdrawn) The electronic system of claim 118, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as an alterable logic device (ALD).

120. (Withdrawn) The electronic system of claim 118, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as a programmable logic device (PLD).

121. (Withdrawn) The electronic system of claim 117, wherein the plurality of fixed threshold devices include an output node, and the plurality of nonvolatile devices are operably coupled to the output node to provide the desired logic functions.

122. (Withdrawn) The electronic system of claim 121, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as an alterable logic device (ALD).

123. (Withdrawn) The electronic system of claim 121, wherein the plurality of fixed threshold devices and the plurality of nonvolatile devices are deployed as a programmable logic device (PLD).

124. (Withdrawn) An electronic system, comprising:

a programmable logic array; and

a nonvolatile programmable memory array (NVPMA) coupled to the programmable logic array, wherein the NVPMA includes a plurality of logic devices, each of the plurality of logic devices including:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

125. (Previously Presented) A gate stack, comprising:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

126. (Previously Presented) A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

127. (Previously Presented) A nonvolatile memory device, comprising:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

128. (Withdrawn) A gate stack, comprising:

a first injector medium;

a tunnel medium disposed on the first injector medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3; and

a second injector medium disposed on the high K charge blocking and charge storing medium.

129. (Withdrawn) A gate stack, comprising:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes silicon-rich Al_2O_3;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

130. (Withdrawn) A gate stack, comprising:

a first injector medium disposed on a substrate;

a tunnel medium disposed on the first injector medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes silicon-rich Al_2O_3;

a high K charge blocking medium stored on the high K charge storing medium; and

a second injector medium disposed on the high K charge blocking medium.

131. (Withdrawn) A memory cell, comprising:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes silicon-rich Al_2O_3;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

132. (Previously Presented) An electronic system, comprising:

a processor; and

a nonvolatile memory device coupled to the processor, the nonvolatile memory device including:

an array of memory cells operably coupled to a grid of row lines and column lines;

row select circuitry for selecting a row of memory cells; and

column select circuitry for selecting a column of memory cells,

wherein the row select circuitry and the column select circuitry cooperate to select a memory cell in the selected row and the selected column for application of a programming voltage; and

wherein each memory cell includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge blocking and charge storing medium disposed on the tunnel medium, wherein the high K charge blocking and charge storing medium includes silicon-rich Al_2O_3; and

an injector medium operably disposed with respect to the tunnel medium and the high K charge blocking and charge storing medium to provide charge transport by enhanced tunneling.

133. (Withdrawn) An electronic system, comprising:

a plurality of fixed threshold devices for performing random logic functions; and

a plurality of nonvolatile devices operably coupled to the plurality of fixed threshold devices to provide desired logic functions, wherein each of the plurality of nonvolatile devices includes:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes silicon-rich Al_2O_3;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.

134. (Withdrawn) An electronic system, comprising:

a programmable logic array; and

a nonvolatile programmable memory array (NVPMA) coupled to the programmable logic array, wherein the NVPMA includes a plurality of logic devices, each of the plurality of logic devices including:

a substrate including diffused regions that form a source region and a drain region;

a gate stack disposed on the substrate between the source region and the drain region; and

a gate disposed on the gate stack,

wherein the gate stack includes:

a tunnel medium;

a high K charge storing medium disposed on the tunnel medium, wherein the high K charge storing medium includes silicon-rich Al_2O_3;

a high K charge blocking medium disposed on the high K charge storing medium; and

an injector medium operably disposed with respect to the tunnel medium, the high K charge storing medium and the high K charge blocking medium to provide charge transport by enhanced tunneling.